Joint Inventors

Docket No. 20061/OF03P197

"EXPRESS MAIL" mailing label No.
EL 995 292 385 US

Date of Deposit: **November 25, 2003**

I hereby certify that this paper (or fee) is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 CFR §1.10 on the date indicated above and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Charissa Wheeler

APPLICATION FOR UNITED STATES LETTERS PATENT

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that We, **Byung Hyun JUNG**, a citizen of the Republic of Korea, residing at 103-903, Keumho apartment, 578, Kwangjang-Dong, Kwangjin-Gu, Seoul, 143-210, Republic of Korea; and **Hyoung Yoon KIM**, a citizen of the Republic of Korea, residing at 321-1401, Jugong apartment, Bunpyoung-Dong, Heungduck-Gu, Cheongju-Si, Choongcheongbuk-Do, Cheongju-Si, 361-201, Republic of Korea have invented a new and useful **METHODS OF MANUFACTURING A SEMICONDUCTOR DEVICE**, of which the following is a specification.

METHODS OF MANUFACTURING A SEMICONDUCTOR DEVICE

FIELD OF THE DISCLOSURE

[0001] The present disclosure relates generally to semiconductor devices and, more particularly, to methods of manufacturing a semiconductor device.

BACKGROUND

[0002] Due to the high integration of semiconductor devices, very small wiring is required. Such small wiring causes an increase in the resistance of the wiring and an increase in the signal transfer delay. To solve the problem of signal transfer delay, a multi-layered wiring structure has been introduced for use instead of the prior single layered wiring structure. In the multi-layered wiring structure, the space between wires is further narrowed. As a result, parasitic capacitance between wires on the same layer is increased and the signal transfer delay is worsened. Particularly, in the case of small line width wiring, the signal transfer delay caused by the parasitic capacitance between wires has a marked effect on an operational feature of the semiconductor device.

[0003] To reduce parasitic capacitance between wires, it is preferable to reduce the thickness of the wires and to thicken an insulating layer. Accordingly, copper having low resistivity is often used as a wiring material and various materials having low permittivity have been proposed as the insulating layer. However, it is difficult to perform a dry etching when copper

is used, since the vapor pressure of etching by-products is low. Therefore, a Damascene process which forms copper wiring by forming a hole (e.g., a via hole or a contact hole) in an insulating layer, filling the hole with copper and planarizing the copper has been used recently.

[0004] For the Damascene process, an etch stopper layer is required to perform a chemical mechanical polishing (CMP) process for planarizing copper. If the permittivity of the etch stopper layer is high, the permittivity of the insulating layer is also increased. Thus, the etch stopper layer should be formed of thin material with low permittivity. A representative layer that is currently commonly used as an etch stopper layer is a silicon nitride layer. However, in the CMP process, when adapting an End Point Detection (EPD) system employing an Optical Emission Spectroscopy (OES) method, the etch stopper layer may be easily etched, since the end point of the etching of the wiring material is detected after the silicon nitride layer, (i.e., the etch stopper layer), has already been exposed. Due to this, if the thickness of the etch stopper layer is thin, the etch stopper layer may be easily broken. Thus, it is preferable to use an EPD system employing laser interferometers. This is because loss of the etch stopper layer can be reduced by terminating the etching of wiring material before the exposure of the etch stopper layer. Thus, since it is possible to use a thin etch stopper layer, the permittivity of the whole insulating layer, including the etch stopper layer, may be reduced.

[0005] In a conventional metallization process using a Dual Damascene process as shown in Figure 1, an insulating layer 11 is deposited on a semiconductor substrate 10, (e.g., a single crystal silicon substrate). A

contact hole 12 is formed in a part of the insulating layer 11 to expose a contact region (not shown) of the semiconductor substrate 10. A copper barrier layer 13 is formed on an inner wall of the contact hole 12, the surface of the contact region, and the insulating layer 11. A copper layer 15 for filling the contact hole 12 is deposited on the copper barrier layer 13. The copper layer 15 of the contact hole 12 is planarized with the insulating layer 11 by a CMP process. Then, a copper barrier layer 17 such as a nitride layer is deposited on the insulating layer 11 and the copper layer 15. An upper insulating layer 19 is deposited on the copper barrier layer 17. An upper contact hole 20 for exposing a contact region of the copper layer 15 is formed in a part of the upper insulating layer 19.

[0006] As shown in Figure 2, before deposition of the copper barrier layer (e.g., Ta or TaN) in the upper contact hole 20, a copper oxide layer (for example, a CuO layer 16), an insulating layer of a surface of the copper layer, is removed by plasma processing using H_2. The CuO layer 16 is parasitically formed on the surface of the copper layer 15 in the course of a wet-treatment of the copper layer 15 for forming the insulating layer 19. The removing process is performed because a contact characteristic of the copper layer 15 and the upper copper layer is deteriorated when a post process for filling the upper contact hole 20 with an upper copper layer (not shown) is performed while leaving the CuO layer 16 as it is.

[0007] However, since the conventional method uses explosive H_2 gas when removing the CuO layer 16, it has a problem in that the stability of

process for removing CuO layer is hardly secured.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figures 1 and 2 illustrate a prior art copper metallization process using a conventional Dual Damascene process.

[0009] Figures 3 to 7 illustrate an example method of manufacturing a semiconductor device using a Dual Damascene process in accordance with the teachings of the disclosure.

[0010] In the following description and drawings, the same reference numerals are used to designate the same or similar components, and so repetition of the description on the same or similar components will be omitted.

DETAILED DESCRIPTION

[0011] The entire disclosure of Korean Patent Application No. 10-2002-0080016 filed on December 14, 2002 is incorporated herein by reference in its entirety.

[0012] Figures 3 to 7 illustrate an example method of manufacturing a semiconductor device . Figure 3 illustrates a semiconductor substrate 10, (for example, a single crystal silicon substrate). It is evident that a gate electrode and a source/drain of a transistor (e.g., for a memory device and/or a logic device) are formed on the semiconductor substrate 10. Then, an insulating layer 11, (such as an oxide layer), is deposited on the semiconductor substrate 10. The insulating layer 11 is then planarized by, for example, a CMP

process. For ease of illustration, the insulating layer 11 is illustrated as a single layered structure, but it can be formed of various materials and have a multi-layered structure to improve a characteristic of the insulating layer.

[0013] After the planarization of the insulating layer 11, a contact hole 12 for exposing a contact region (not shown) of the semiconductor substrate 10 is formed in the insulating layer 11 by photolithography to enable performance of a Dual Damascene process. Then, a copper barrier layer 13, (for example, Ta or TaN), is deposited on the insulating layer 11 and in the contact hole 12. Then, using, for example, an electrolysis method, the contact hole 12 is filled with a copper layer 15. Using, for example, a CMP process, the copper layer 15 in the contact hole 12 is planarized with the insulating layer 11.

[0014] At this time, it is preferable that the copper barrier layer 13 and the copper layer 15 are not left on the insulating layer 11 outside the contact hole 12, but instead, are only left in the contact hole 12. Also, since a wet process is added to the CMP process, an insulating layer (e.g., a CuO layer 16, (i.e., a copper oxide layer)), is parasitically formed on the planarized\surface of the copper layer 15 as shown in Figure 3. The CuO layer 16 deteriorates a contact characteristic of the copper layer 15 and an upper copper layer 39 (shown in Figure 7), so the CuO layer 16 should be removed before filling an upper contact hole with the upper copper layer 39.

[0015] Referring to Figure 4, the semiconductor substrate 10 is mounted in a reaction chamber (not shown) for depositing, for example, a nitride layer 31 (see Figure 5), for depositing a copper barrier layer 33 (see

Figure 6), and for removing the CuO layer 16 of Figure 3. The CuO layer 16 is completely removed by plasma processing using NH_3 or N_2, thus exposing the copper layer 15.

[0016] Preferably, the temperature of the reaction chamber for plasma processing is maintained at about 300 to 500 ℃, and the flow rate of the NH_3 or N_2 gas injected into the reaction chamber is maintained at about 100 to 200 sccm. To remove the CuO layer 16 from the copper layer 15, the semiconductor substrate 10 can be heat-treated in a conventional furnace (not shown). Preferably, the temperature of the furnace is maintained at about 400 to 600 ℃, and the flow rate of the NH_3 or N_2 gas injected into the furnace is maintained at about 5 to 20 slm during this heat treatment process.

[0017] Accordingly, the stability of the process for removing the CuO layer in the reaction chamber is secured by performing plasma processing using NH_3 or N_2 gas with little explosive possibility, instead of performing a conventional plasma processing using H_2 to remove the CuO layer 16.

[0018] Also, after the plasma processing or the heat treatment for removing the CuO layer 16 is completed, as shown in Figure 5 a conductive copper nitride layer, (i.e., a CuN layer 31), is formed in a thickness of about 50 to 200 Å on the surface of the copper layer 15. The inclusion of this copper nitride layer 31 considerably reduces the thickness of the nitride layer 33 of Figure 6 (which is deposited in a subsequent process).

[0019] Referring to Figure 6, a copper barrier layer 33 (e.g., the nitride layer 33) having a high dielectric constant k is successively deposited in a thin thickness of about 100 to 500 Å on the insulating layer 11 and on the CuN

layer 31 without time delay, while leaving the semiconductor substrate 10 as it is.

[0020] As shown in Figure 5, since the copper barrier layer 31 has already been formed on the copper layer 15, a thinner nitride layer 33 can be deposited as compared to the nitride layer 33 required in the conventional process. The use of this thinner nitride layer 33 prevents degradation of the operational velocity of the semiconductor device due to an increase of the dielectric constant between the insulating layers.

[0021] Referring to Figure 7, an upper insulating layer 35, (e.g., an oxide layer), is deposited on the nitride layer 33. The upper insulating layer 35 is planarized by, for example, a CMP process. For ease of illustration, the upper insulating layer 35 is illustrated as a single layered structure, but persons of ordinary skill in the art will readily appreciate that it can be formed of various materials and have a multi-layered structure to improve a characteristic of the insulating layer 35.

[0022] An upper contact hole 37 for exposing a contact region (not shown) of the copper layer 15 is formed in the upper insulating layer 35 and the nitride layer 33 by photolithography to enable performance of a Dual Damascene process. Since the CuN layer 31 on the copper layer 15 functions as an etch stopper layer, the copper layer 15 is, in fact, not exposed. As a result, generation of a CuO layer 16 on the copper layer 15 is prevented even when the upper contact hole 36 is formed.

[0023] A copper barrier layer 37, (e.g., Ta or TaN), is deposited on the upper insulating layer 35 and in the upper contact hole 36. Then, using, for

example, an electrolysis method, the upper contact hole 36 is filled with an upper copper layer 39. Using, for example, a CMP process, the upper copper layer 39 in the upper contact hole 36 is planarized with the upper insulating layer 35. The copper barrier layer 37 and the upper copper layer 39 are preferably not left on the upper insulating layer 35 outside the upper contact hole 36, but are preferably only left in the upper contact hole 36.

[0024] The stability of the process for removing the CuO layer 16 is secured and a contact characteristic of the semiconductor device is improved by performing plasma processing using NH_3 or N_2 gas with little explosive possibility, instead of performing a conventional plasma processing using explosive H_2 gas to remove the CuO layer 16 that is parasitically formed on the copper layer 15. Furthermore, a high dielectric constant nitride layer 33 is thinly formed on the copper layer 15 to thereby increase the operational velocity of the semiconductor device, by forming the CuN layer 31 on the copper layer 15 while removing the CuO layer 16.

[0025] From the foregoing, persons of ordinary skill in the art will appreciate that the disclosed methods achieve process simplification and improve productivity because removal of the CuO layer 16, formation of the CuN layer 31 and deposition of the nitride layer 33 can be performed in the same single reaction chamber.

[0026] As described above, the illustrated method of manufacturing semiconductor devices is performed using a Damascene process. The contact hole 12 of the insulating layer 11 is filled with the copper layer 15 and, then, the copper layer 15 is planarized. During the planarizing, the CuO layer 16 is

parasitically formed on the surface of the copper layer 15. The CuO layer 16 is removed by plasma processing using ammonia or nitrogen. The conductive CuN layer 31, (i.e., the copper barrier layer), is formed on the surface of the copper layer 15. The nitride layer 33, (i.e., the copper barrier layer for the copper layer), is deposited on the insulating layer 11 and the CuN layer 31. Then, the upper insulating layer 35 is deposited on the nitride layer 33, and the upper contact hole 36 is formed in the upper insulating layer 35 and the nitride layer 33 to expose the copper layer 15. Then, the upper contact hole36 is filled with the upper copper layer 39 and the upper copper layer 39 is planarized.

[0027] Accordingly, the CuO layer 16 is removed and the CuN layer 31 is formed by plasma processing using ammonia or nitrogen, thus securing the stability of the removal process of the CuO layer 16 and preventing degradation of a contact characteristic of the semiconductor device. Furthermore, the nitride layer 33 (which has a high dielectric constant) can be deposited more thinly on the copper layer 15, thus increasing the operational velocity of the semiconductor device. Also, removal of the CuO layer 16, formation of the CuN layer 31, and deposition of the nitride layer 33 are conducted in the same single reaction chamber, thus providing process simplification and increasing productivity.

[0028] From the foregoing, persons of ordinary skill in the art will appreciate that methods of manufacturing a semiconductor device have been provided. The disclosed methods secure the stability of the process for removing a CuO layer 16 from a copper layer 15 while maintaining a contact

characteristic of the copper layer 15 and an upper copper layer 39. Further, the disclosed methods increase the operational velocity by reducing a thickness of the nitride layer 33 between the upper and lower layers.

[0029] A disclosed method of manufacturing a semiconductor devicecomprises: forming a contact hole 12 in an insulating layer11; filling the contact hole 12 with a copper layer 15; planarizing the copper layer 15; removing a copper oxide layer 16 parasitically formed on the surface of the copper layer 15; depositing a copper barrier layer 33 on the insulating layer 11 and the copper layer 15; depositing an upper insulating layer 35 on the copper barrier layer 33; and forming an upper contact hole in the copper barrier layer 33 and the upper insulating layer 35 so as to expose the copper layer15.

[0030] Although certain example methods and apparatus have been described herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers all methods, apparatus and articles of manufacture fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.